

Presentation Schedule

Session – 1 (Digital Design & Embedded Systems)		
Paper ID	Title	Authors
NCVSC 202	Design and Implementation of Vision System by Matched Filter Algorithm on a FPGA	K.Cholan
NCVSC 204	Proposed Evolvable Unit for 2-Bit Adder Using Genetic Algorithm	Vedavathi.A, Gayatri.Malhotra Meena. K.V
NCVSC 208	Transistor Realization of Reversible Parallel Adder/Subtractor	Kavyasree.B, Y.Syamala and K.Srilakshmi
NCVSC 209	Power Reduction in Memory ECC Checkers by using Genetic Algorithm	Sharath Chandra Inguva
NCVSC 403	Effective Navigation for Visually Impaired by Wearable Obstacle Avoidance System	S.Bharathi, S.Vivek & J.Vinoth kumar
NCVSC 411	Voice Recognition Based Wireless Home Automation System	P.Narasaiyah, Y.Usha Devi
Session – 2 (Image Processing)		
Paper ID	Title	Authors
NCVSC 109	Performance Analysis of Balanced Gray codes for MPSK Signals	K.Usha Kamle K. Jaya Sankar
NCVSC 303	Image Denoising: A Two Stage Implementation Using Principal Component Analysis With Local Pixel Grouping	G.Srivathsa, Ch.Ravi Srinivas
NCVSC 307	Image Encryption Using Binary Parity Check Method	Basanta kumar Sahu, Y.E.Vasanth kumar
NCVSC 311	Implementation of Low Power Frame Synchronizer And Code Group Detector For 3g Asynchronous W-CDMA System	M.Kamaraju, P.Pavan
NCVSC 313	Object detection using fast corner based on CDPA Technique	Y.Madhuri, O.siva sowmya, G.V.N Sravya., B.Bhanuprakash. & Irphan ali shaik
NCVSC 314	Performance of Semi-Blind Reference Watermarking Scheme Using DWT-SVD for Copyright Protection	Saryanarayana Murty.P, Lakshmi.V, Rajesh Kumar.P
Session – 3 (Image Processing)		
Paper ID	Title	Authors
NCVSC 331	Fingerprint Image Enhancement Using Fuzzy Logic Based Pi-Membership Function	M.Suneel, ² K.Udayam, ³ D.Rajendra Prasad, ⁴ K.Kiran Kumar
NCVSC 733	An Optimization Technique (PSO) for The Design of Optimal Digital Fir Low Pass Differentiator	Sambaiah Pelluri Venkatappareddy.P
Session – 4 (Communications & Digital Signal Processing)		
Paper ID	Title	Authors
NCVSC 101	A Priority Based Routing Algorithm and Wavelength Assignment problem for Wavelength Division multiplexing in optical networks	M.Rangaswamy K.Aparna
NCVSC 103	Future Wireless Cellular Systems	J.Umesh Rao S.Rameshbabu G.Mahesh
NCVSC 105	LMS Based Channel Equalization	Chittibabu.Yezarla M.John Joseph
NCVSC 114	Implementation of different Codes for Base Band Wireless Communication Systems	Subrahmanyam.Ch. Madala Lakshmi Tulasi, Avula Priyanka
NCVSC 115	Modulation and Simulation Of Fading Channels	Subrahmanyam.Ch, K.Neelima Binitha Thomas
NCVSC 123	Power Consumption mechanisms based on QoS and QoE for Wireless Devices	K.Prasuna, M.Padmaja
NCVSC 137	Vertical Handoff Decision between WLAN and Cellular Networks Based on RSS Averaged and Lifetime Estimation	Priya Govind Bhagat, Sonali Pramod Badgujar, Sneha Vishnu Bantu Prof. Sahana Bhosale
Session – 5 (Communications & VLSI)		
Paper ID	Title	Authors
NCVSC 138	Analysis Of Probability Of Handover Failure During Vertical Handoff Between Cellular Network And WLANs	Poonam Jaswani , Pranjali Bhandari, Shivani Singh, Sahana Bhosale,R.Daruwala
NCVSC 140	Design of CODEC to avoid crosstalk in On-Chip Bus	T. Swetha, Rajesh Akula

NCVSC 310	An Adaptive Fuzzy C-Means Clustering Algorithm for Breast Image Segmentation	Tara.saikumar P.SreenivasaMurthy
NCVSC 604	Performance Of Turbo Decoding Algorithms at Low SNR	P.Surendra Kumar M.Rajani Devi, T.Krishna Chaitanya
NCVSC 702	Design And Implementation of Floating Point Arithmetic for Analog Modeling	R.Prakash Rao, Dr.B.K.Madhavi
NCVSC 703	Design And Implementation of Simultaneous Shield and Repeater Insertion for On-Chip Interconnects	M.Surendra goud, Mr.Y.Sreenivas goud
NCVSC 722	Resistive Feedback CMOS Low Noise Amplifiers for Multiband Applications	Sambaiah Pelluri Venkatappareddy.P
Session – 6 (VLSI, MEMs, Fuzzy Logic & Nano Technology)		
Paper ID	Title	Authors
NCVSC 705	Design Of Low Power 4-Bit Full Adder using Sleepy Keeper Approach	B.Muralikrishna, K.Gnana Deepika
NCVSC 706	Efficient Design Of Reversible Bi-Directional Barrel Shifter	Satish Paid, Rohit Sreerama, K.Cholan
NCVSC 709	Recursive Bisection Based Mixed Block Placement For VLSI Design	R.Prabhakar, Dr K E Sreenivasa Murthy Dr K Soundara Raj
NCVSC 714	Efficient VLSI Implementation of High Speed Low-Density Parity-Check Code Decoder using Min-Sum Algorithm	Pratik Ganguly, Rahul .S
NCVSC 719	Area Efficient Maximum Likelihood FPGA Based Viterbi Decoder	Ch.S.Srivalli, N.Usha Rani
NCVSC 721	Performance Analysis of Modfet LNA	V.J.K.Kishor Sonti, V.Kannan