20ES006 - Hardware Software Co-Design

UNIT I
Issues in Co-Design and Synthesis Algorithms: Co- Design Models, Architectures, anguages, A Generic Codesign Methodology. Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT II
Prototyping & Emulation and Target Architectures: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure, Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT III
Compilation Techniques and Tools for Embedded Processor Architectures: Modern embedded architectures, embedded software development needs, compilation technologies practical consideration in a compiler development environment. **Design Specification and Verification:** Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification.

UNIT IV
Languages for System-Level Specification and Design I: System – level specification, design representation for system level synthesis, system level specification languages,

UNIT V
Languages for System-Level Specification And Design-II: Heterogeneous specifications and multi language co-simulation. Introduction to Cosyma system and LYCOS system.

TEXT BOOKS:
1. Jorgen Staunstrup, Wayne Wolf, "Hardware / software co- design Principles and Practice", Springer, 2009.
2. Kluwer, "Hardware / software co- design Principles and Practice", academic publishers,2002.

Hardware Software Co-Design Lab Experiments
(Xilinx FPGA Based and Embedded Processor)

1. Study of FPGA-based Embedded Processor, Hardware–Software Task Partitioning, FPGA Fabric Immersed Processors and Soft Processors vs Hard Processors.
2. Study of tool Flow for Hardware–Software Co-design
3. Interfacing Memory to the Processor
4. Interfacing Processor with Peripherals
5. Study of types of On-chip Interfaces: Wishbone Interface, Avalon Switch Matrix, OPB Bus Interface
6. Interfacing a Robot Axis Position Control to processor

FPGA-based Signal Interfacing and Conditioning

7. Interfacing FPGA with Serial Data Communication
8. Interfacing FPGA with Physical Layer for Serial Communication
9. Interfacing FPGA with RS-232-based Point-to-Point Communication

10. Interfacing FPGA with RS-485-based Multi-point Communication
11. Interfacing FPGA with Serial Peripheral Interface (SPI)

Signal Conditioning with FPGAs

12. Interfacing Stepper Motor Using FPGA
13. Interfacing Permanent Magnet DC Motor Using FPGA
14. Interfacing Brushless DC Motor Using FPGA

Prototyping Using FPGA

15. Study of FPGA Design Test Methodology
16. UART for Software Testing
17. Study of FPGA Hardware Testing Methodology

Reference Books:

1. 1.Rahul Dubay Introduction to Embedded System Design Using Field Programmable Gate Arrays, 2009 Springer-Verlag London Limited.

2. Frank Vahid & Tony Givargis, Embedded System Design, A Unified Hardware/Software Introduction, ISBN 978-0-471-38678-0 2014.