20ES010 - Programmable Logic Embedded System Design

UNIT – I

Introduction- System tradeoffs and evolution of ASIC Technology- System on chip concepts and methodology – SoC design issues -SoC challenges and components.

UNIT – II

Design Methodological For Logic Cores- SoC Design Flow – On-chip buses –Design process forhardcores–Softandfirmcores–CoreandSoCdesignexamples.

UNIT – III

Design Methodology for Memory and Analog Cores- Embedded memories –Simulation modes Specification of analog circuits – A to D converter –Phase locked loops –High I/O.

UNIT – IV

Design Validation- Core level validation –Test benches –SoC design validation – Co simulation –hardware/ Software co-verification. Case Study: Validation and test of systems on chip.

UNIT – V

SoC Testing- SoC Test Issues –Cores with boundary scan –Test methodology for design reuse– Testing of microprocessor cores – Built in self-method –testing of embedded memories. Case Study: Integrating BIST techniques for on-line SoC testing.

TEXTBOOKS:

1. RochitRajsunah,System-on-a-chip:DesignandTest,ArtechHouse,2007.
2. PrakashRaslinkar,PeterPaterson&LeenaSingh,System-on-a-chipverification:Methodology and Techniques, Kluwer Academic Publishers,2000.

REFERENCE BOOKS:

1. M.Keating, D.Flynn, R.Aitken, A, GibbonsShi, Low Power Methodology Manual for System- on-ChipDesignSeries:IntegratedCircuitsandSystems,Springer,2007.
2. L.Balado, E. Lupon, Validation and test of systems on chip, IEEE conference on ASIC/ SOC,1999.
3. A.Manzone,P.Bernardi,M.Grosso,M.Rebaudengo,E.Sanchez,M.SReorda,CentroRicerch e Fiat, Integrating BIST techniques for on-line SoC testing, IEEE Symposium on On-Line testing,2000.