20ES017 - DSP Processors

UNIT–I **L-09**

ARCHITECTURESFORPROGRAMMABLEDIGITALSIGNALPROCESSINGDEVICES: Introduction, Basic Architectural Features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External Interfacing.

UNIT–II **L-09**

PROGRAMMABLE DIGITAL SIGNAL PROCESSORS : Introduction, Commercial Digital Signal- processing Devices, Data Addressing Modes of TMS320C54xx Digital Signal Processors, Data Addressing Modes of TMS320C54xx Processors, Memory Space of TMS320C54xx Processors, Program Control.

UNIT–III **L-09**

DSPPROGRAMMINGANDOPERATIONS:TMS320C54xxInstructionsandProgramming, Pro- gramming for IIR, FIR, FFT etc., On-Chip peripherals, Interrupts of TMS320C54xx Processors, Pipeline Operation of TMS320C54xxProcessors.

UNIT–IV **L-09**

INTERFACINGMEMORYANDPARALLELI/OPERIPHERALSTOPROGRAMMABLEDSP DEVICES:

Introduction, Memory Space Organization, External Bus Interfacing Signals, Memory Interface, Parallel I/O Interface, Programmed I/O, Interrupts and I/O, Direct Memory Access (DMA)

UNIT–V **L-09**

INTERFACINGSERIALCONVERTERSTOAPROGRAMMABLEDSPDEVICE: Introduction,Syn-chronousSerialInterface,Amulti-channelBufferedSerialPort(McBSP),McBSPProgramming,A CODEC Interface Circuit, CODEC Programming, A CODEC-DSP Interface Example

TEXTBOOKS:

1. Lapsley et al., “DSP Processor Fundamentals, Architectures & Features”, S. Chand & Co, 2000.
2. “DigitalSignalProcessing”, A.Singh & S.Srinivasan, Thomson Learning.

REFERENCE BOOKS:

1. B. VenkataRamani and M. Bhaskar, “Digital Signal Processors, Architecture, Programming and Applications”, TMH,2004.
2. JonathamStein,“DigitalSignalProcessing”,JohnWiley,2000.
3. Embedded Dsp Processor Design Application Specific Instruction Set Processors by LiuShroff(2008).