20ES020 - Design of Fault-tolerant Systems

UNIT- I

Fault Tolerant Design: Basic concepts: Reliability concepts, Failures & faults, Reliability and Failure rate, Relation between reliability and mean time between failure, maintainability and availability, reliability of series, parallel and parallel-series combinational circuits. Fault Tolerant Design: Basic concepts-static, dynamic, hybrid, triple modular redundant system (TMR), 5MR reconfiguration techniques, Data redundancy, Time redundancy and software Redundancy concepts. [TEXTBOOK-1]

UNIT- II

Self Checking circuits & Fail safe Design: Self Checking Circuits: Basic concepts of self checking circuits, Design of Totally self checking checker, Checkers using m out of n codes, Berger code, Low cost residue code. Fail Safe Design: Strongly fault secure circuits, fail safe design of sequential circuits using partition theory and Berger code, totally self checking PLA design. [TEXTBOOK-1]

UNIT- III

Design for Testability: Design for testability for combinational circuits: Basic concepts of Testability, Controllability and observability, The Reed Muller's expansion technique, use of control and syndrome testable designs.

Design for testability by means of scan: Making circuits Testable, Testability Insertion, Full scan DFT technique- Full scan insertion, flip-flop Structures, Full scan design and Test, Scan Architecturesfull scan design, Shadow register DFT, Partial scan methods, multiple scan design, other scan designs

UNIT- IV

Logic Built-in-self-test: BIST Basics-Memory-based BIST,BIST effectiveness, BIST types, Designing a BIST, Test Pattern Generation-Engaging TPGs, exhaustive counters, ring counters, twisted ring counter, Linear feedback shift register, Output Response Analysis-Engaging ORA's, One's counter, transition counter, parity checking, Serial LFSRs, Parallel Signature analysis, BIST architectures-BIST related terminologies, A centralized and separate Board-level BIST architecture, Built-in evaluation and self test(BEST), Random Test socket(RTS), LSSD On-chip self test, Self – testing using MISR and SRSG, Concurrent BIST, BILBO, Enhancing coverage, RT level BIST design CUT design, simulation and synthesis, RTS BIST insertion, Configuring the RTS BIST, incorporating configurations in BIST, Design of STUMPS, RTS and STUMPS results. [TEXTBOOK-2]

UNIT- V

Standard IEEE Test Access Methods: Boundary Scan Basics, Boundary scan architecture- Test access port, Boundary scan registers, TAP controller, the decoder unit, select and other units, Boundary scan Test Instructions-Mandatory instructions, Board level scan chain structure-One serial scan chain, multiple-scan chain with one control test port, multiple-scan chains with one TDI,TDO but multiple TMS, Multiple-scan chain, multiple access port, RT Level boundary scan-inserting boundary scan test hardware for CUT, Two module test case, virtual boundary scan tester, Boundary Scan Description language. [TEXTBOOK-2]

TEXT BOOKS:

1. Parag K. Lala, “Fault Tolerant & Fault Testable Hardware Design”, 1984, PHI
2. Zainalabedin Navabi, “Digital System Test and Testable Design using HDL models and Architectures”, Springer International Edition.

REFERENCES:

3. Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman, “Digital Systems Testing and Testable Design”, Jaico Books
4. Bushnell & Vishwani D. Agarwal, “Essentials of Electronic Testing”, Springer.
5. Alfred L. Crouch, “Design for Test for Digital IC’s and Embedded Core Systems”, 2008, Pearson Education.

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