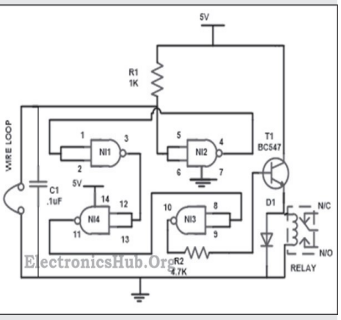


***Source:***
*https://cdn.sparkfun.com/assets/*

# 19CS204 DIGITAL LOGIC DESIGN

Hours Per Week :

| L | T | P | C |
|---|---|---|---|
| 3 | - | - | 3 |

Total Hours :

| L | T | P |
|---|---|---|
| 45 | - | - |

| CS | WA/RA | SSH | SA | S | BS |
|---|---|---|---|---|---|
| 5 | 5 | 30 | 20 | 5 | 5 |

## COURSE DESCRIPTION AND OBJECTIVES:

This course introduces the basic knowledge on number systems, analysis and design of combinational and sequential circuits. The course mainly focuses on designing digital circuits in optimized manner by using components like decoders, encodes, multiplexers. It also deals with design of sequential circuits and Programmable logic devices.

## COURSE OUTCOMES:

Upon completion of the course, the student will be able to achieve the following outcomes:

| COs | Course Outcomes | POs |
|---|---|---|
| 1 | Understand the basic digital logic fundamentals such as number system, binary codes and complements. | 1 |
| 2 | Apply Boolean algebra rules and karnaugh map method to reduce the Boolean functions. | 1 |
| 3 | Design various types of combinational and sequential circuits and improve the performance by reducing the complexities. | 3 |
| 4 | Analyze and differentiate various types of Programmable Logic Devices. | 2 |

## SKILLS:

- ✓ *Design of logical circuits using all types of gates.*
- ✓ *Minimizing of Boolean functions.*
- ✓ *Design of simple logical circuits.*
- ✓ *Design of different types of counters.*

**UNIT– I** **L- 9**

**DIGITAL SYSTEMS AND BINARY NUMBERS-** Digital systems; Binary numbers; Number base conversions; Octal and hexa decimal numbers; Complements of numbers; Signed binary numbers; Binary codes; Boolean algebra - basic definitions; Axiomatic definition of boolean algebra; Basic theorems and properties of boolean algebra.

**UNIT – II** **L- 9**

**LOGIC GATES AND GATE-LEVEL MINIMIZATION**: Boolean functions; Canonical and standard forms; Other logic operations; Digital logic gates; The map method - four variable K map; POS and SOP simplification; Don't care conditions; NAND and NOR implementation;Other two level implementations.

**UNIT – III** **L- 9**

**COMBINATIONAL LOGIC**: Introduction - combinational circuits analysis, design procedure; Binary adder subtractor; Binary increment; Decimal adder; Binary multiplier; Magnitude comparator; Decoders; Encoders; Multiplexers; De-Multiplexer.

**UNIT – IV** **L- 9**

**SYNCHRONOUS SEQUENTIAL LOGIC**: Sequential circuits; storage elements - latches, flip flops; Analysis of sequential circuits; Design procedure; Flipflop conversion; Registers; Ripple counters; Synchronous counters.

**UNIT - V** **L- 9**

**MEMORY AND PROGRAMMABLE LOGIC:** Intraduction; Random access memory; Memory decoding; Read only memory; Programmable logic array; Programmable array logic.

## TEXT BOOK:

1. M Morris Mano and Michael D. Ciletti, "Digital Design", 5th edition, Pearson Education, 2013.

## REFERENCE BOOKS:

1. H Taub and D Schilling, "Digital Integrated Electronics", 2nd edition, TataMc Graw-Hill, 2004.
2. Z. Kohavi, "Switching and Finite Automata Theory", 2nd edition, Tata McGraw-Hill, 2008.